EE214 - Digital Circuits Lab

Encoders

Thursday Batch

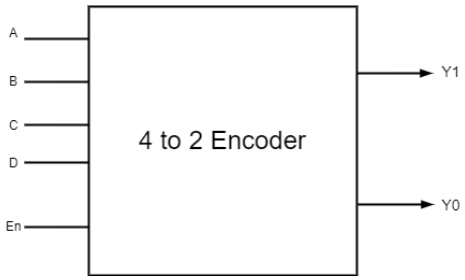
11/08/2022

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.
5. Demonstrate the simulations to your TA
6. Submit the entire project files in .zip format in Moodle.

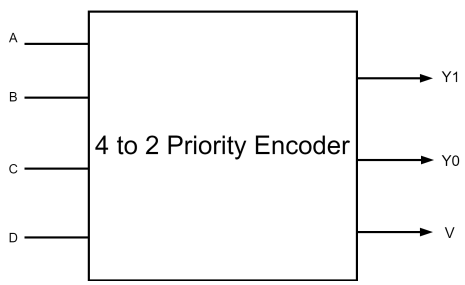
Problem Statement:

1. **Part-A: 4 to 2 encoder**
   (a) Design: Design a 4 to 2 encoder with enable input as shown in figure below. Use only two input gates and inverters given in Gates.vhdl. (Assume enable as active high input). [3 Marks]
   INFO: Encoders are combinational circuit which takes in binary information in the form of 2^N input lines and encode the binary information into N output lines. Hint: See Tracefile to understand the functionality of encoder



   (b) VHDL description: Describe a 4 to 2 encoder with enable input in VHDL. [5 Marks]
   (c) Simulation: Simulate the encoder using the generic testbench to confirm the correctness of your description. [5 Marks]
   NOTE: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< A\ B\ C\ D\ En >\ \ < Y1\ Y0 >\ \ 11$) Tracefile

2. **Part-B: 4 to 2 priority encoder**
   (a) Design: Design a 4 to 2 priority encoder with valid output as shown in figure below. Use only two input gates and inverters given in Gates.vhdl. No need to use enable input. [3 Marks]
   Hint: See Tracefile to understand the functionality of 4 to 2 priority encoder



(b) VHDL description: Describe a 4 to 2 priority encoder with valid output. [5 Marks]
(c) Simulation: Simulate the priority encoder using the generic testbench to confirm the correctness of your description. [5 Marks]
NOTE: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
Tracefile format: ($< A\ B\ C\ D >$ $< Y1\ Y0\ V >$ 111) Tracefile

Part-C: 8 to 3 encoder

(a) Design: Design a 8 to 3 encoder with enable input using 4 to 2 encoder designed in part A and additional two input OR gates given in Gates.vhdl. [3 Marks]
(b) VHDL description: Describe a 8 to 3 encoder with enable input in VHDL using 4 to 2 encoder of part A and additional OR gates given in Gates.vhdl. [5 Marks]
INFO: $2^3 = 8$ data input, 1 enable input, 3 output lines
(c) Simulation: Simulate the 8 to 3 encoder using the generic testbench to confirm the correctness of your description. [5 Marks]
To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
Tracefile format: ($< Y7\ Y6\ Y5\ Y4\ Y3\ Y2\ Y1\ Y0\ E >$ $< A2\ A1\ A0 >$ 111) Tracefile