EE214 Digital Circuits Laboratory
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Problem set: 1 Date: August 11, 2023

Designing Circuits using Universal Gate NOR

Instructions:

1. NOR is a universal gate.
2. For writing VHDL description, use the NOR gate provided in Gates.vhdl (which has been provided in Resource Files).
3. Do pen paper design, use proper labeling for each wire and use the same labels in the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.

Problem Statement:

1. Design and describe AND gate, XOR gate, OR Gate using NOR gate in VHDL using Structural modeling.
2. Design Half Subtractor and Full Subtractor using NOR gates (pen-paper design).
3. Describe Half Subtractor(X-Y) and Full Subtractor(X-Y-B) using NOR gates in VHDL using Structural modeling (use the XOR gate that you have designed using NOR gates). Here X, Y are input bits and borrow bit is represented by input bit B for Full Subtractor.
4. Verify the working of your design by performing RTL simulation using the given tracefile and testbench.

NOTE:

- TRACEFILE for AND gate: AND_Tracefile
  Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for OR gate: OR_Tracefile
  Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for XOR gate: XOR_Tracefile
  Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for Half Subtractor: Half_Subtractor_Tracefile
  Format: Input{X Y} Output{Difference Borrow} MASK{1 1}
- TRACEFILE for Full Subtractor : Full_Subtractor_Tracefile
  Format: Input{X Y B} Output{Difference Borrow} MASK{1 1}