NPTEL Digital Circuits Workshop
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

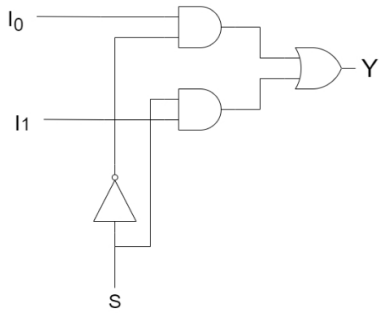
Problem set: 2 Date: August 18, 2023

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA.

Problem Statement:

1. **Part-A: 2x1 Mux**
   (a) VHDL description: Write the VHDL description of a 2x1 multiplexer as shown in figure below.
   INFO: Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output lines.



   (b) Write Truth table and boolean expression for output Y.

   (c) Simulation: Simulate the 2x1 multiplexer using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.
   Tracefile format: $(< In1 >< In0 >< S > \quad < Y > \quad 1)$ Tracefile

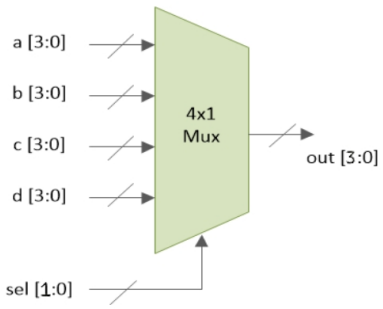
2. **Part-B: 4x1 Mux**
   (a) Design: Design 4x1 Mux using only 2x1 Mux
   INFO: $2^2 =$ 4 data inputs, 2 select lines, 1 output line

   (b) VHDL description: Write the VHDL description of a 4x1 multiplexer designed using 2x1 Mux.

   (c) Simulation: Simulate the 4x1 multiplexer using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: $(< In4 >< In3 >< In2 >< In1 >< S2 >< S1 > \quad < Y > \quad 1)$ Tracefile

3. **Part-C: 4-bit 4x1 Mux**

   (a) Design: Design 4-bit wide 4x1 Mux using only 4x1 Mux designed in part B.



   (b) VHDL description: Write the VHDL description of a 4-bit wide 4x1 multiplexer designed using 4x1 Mux.

   (c) Simulation: Simulate the 4-bit 4x1 multiplexer using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.
   Tracefile format:
   ($d3\ d2\ d1\ d0 >< c3\ c2\ c1\ c0 >< b3\ b2\ b1\ b0 >< a3\ a2\ a1\ a0 >< sel1\ sel0 > \quad < Y3\ Y2\ Y1\ Y0 > \quad 1111$)
   Tracefile