EE214 Digital Circuits Laboratory
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Problem set: 2 Date: August 16, 2023

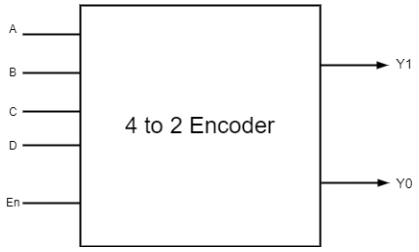
Designing Encoders

Instructions:

1. Use **structural** modelling for this experiment; i.e. instantiating components and using port map to establish the connection between those components.
2. Do pen paper design of the circuit using proper labelling for each wire and use the same labels for the VHDL code.
3. Perform RTL simulation using the provided testbench and TRACEFILE to verify the design.

Problem Statement:

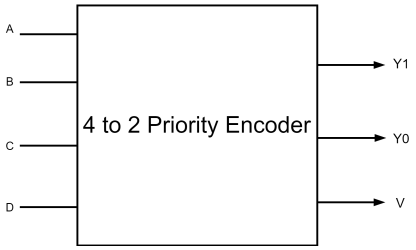
1. **Part-A: 4 to 2 encoder**
   (a) Design: Design a 4 to 2 encoder with enable input as shown in figure below. Use only two input gates and inverters given in Gates.vhdl. (Assume enable as active high input).
   About Encoders: Encoders are the combinational circuits which take in binary information in the form of 2^N input lines and encode the binary information into N output lines.
   Hint: See Tracefile to understand the functionality of encoder.



   (b) VHDL description: Describe a 4 to 2 encoder with enable input in VHDL.
   (c) Simulation: Simulate the encoder using the generic testbench to confirm the correctness of your description.
   Note: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< A\ B\ C\ D\ En >$ $< Y1\ Y0 >$ 11) Tracefile

2. **Part-B: 4 to 2 priority encoder**

   (a) Design: Design a 4 to 2 priority encoder with valid output as shown in figure below. Use only two input gates and inverters given in Gates.vhdl. No need to use enable input.
   Hint: See Tracefile to understand the functionality of 4 to 2 priority encoder



   (b) VHDL description: Describe a 4 to 2 priority encoder with valid output.

   (c) Simulation: Simulate the priority encoder using the generic testbench to confirm the correctness of your description.
   Note: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< A\ B\ C\ D >$ $< Y1\ Y0\ V >$ 111) Tracefile

Part-C: 8 to 3 encoder

   (a) Design: Design an 8 to 3 encoder with enable input using 4 to 2 encoder designed in part A and additional two input OR gates given in Gates.vhdl.

   (b) VHDL description: Describe an 8 to 3 encoder with enable input in VHDL using 4 to 2 encoder of part A and additional OR gates given in Gates.vhdl.
   Note: 8 to 3 encoder has 8-bit input data, one enable input and 3-bit output data

   (c) Simulation: Simulate the 8 to 3 encoder using the generic testbench to confirm the correctness of your description.
   To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< Y7\ Y6\ Y5\ Y4\ Y3\ Y2\ Y1\ Y0\ E >$ $< A2\ A1\ A0 >$ 111) Tracefile