



Fibonacci Detector

Instructions

1. Use Structural modelling for this experiment (use process statement) .
2. Perform RTL simulation using the provided testbench and tracefile.
3. Use the Xen-10 Board to check your model by doing pin planning.

Design

Design a system that detects Fibonacci number. Any number between 0 to 31 will be given as input to the system which will be represented in binary form such as $0 \rightarrow 00000$, $1 \rightarrow 00001$ and so on. The output of the system will be '1' only when the given input is a Fibonacci number.

Show the pen-paper design using K-Maps to the corresponding evaluating TAs.

VHDL Description

Write a VHDL description for the given problem statement.

Inputs(4-bit): $x_4x_3x_2x_1x_0$

Output(1-bit): y

Tracefile format: $\langle x_4x_3x_2x_1x_0 \rangle \quad \langle y \rangle \quad 1$

Design Verification

- Perform RTL Level Simulation of the Fibonacci number detector using the generic testbench to confirm the correctness of your description using the [TRACEFILE](#)
- Perform manual verification using Xen-10 board and verify your design.

- **PIN PLANNING:**

$$x_4 \Rightarrow SW_5 \parallel x_3 \Rightarrow SW_4 \parallel x_2 \Rightarrow SW_3 \parallel x_1 \Rightarrow SW_2 \parallel x_0 \Rightarrow SW_1$$
$$y \Rightarrow LED1$$