



## Prime Number Detector

### Instructions

1. Use structural modelling for this experiment i.e. instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.
5. Perform manual verification using xen-10 board.
6. Demonstrate the experiment to your TA.
7. Submit the entire project files in .zip format in Moodle.

### Design

Design a system that detects a prime number. Any number between 0 to 31 will be given as input to the system which will be represented in binary form such as  $0 \rightarrow 00000$ ,  $1 \rightarrow 00001$  and so on. The output of the system will be '1' only when the given input is a prime number. Show the pen-paper design using K-Maps to the corresponding evaluating TAs.

### VHDL Description

Write a VHDL description for the given problem statement.

Inputs(5-bit):  $x_4x_3x_2x_1x_0$

Output(1-bit):  $y$

Tracefile format:  $\langle x_4x_3x_2x_1x_0 \rangle \quad \langle y \rangle \quad 1$

### Design Verification

- Perform RTL Level Simulation of the prime detector using the generic testbench to confirm the correctness of your description using the [TRACEFILE](#)
- Pin plan switches S5 to S1 as input and LED 8 as output and show the correctness of the design on board.

### Testing on Board

- Test the correctness of your design on the Xen-10 board.
- Perform the pin mapping as follows:

$$\begin{aligned}x_4-x_0 &\implies SW5-SW1; \\ y &\implies LED8\end{aligned}$$