EE214 Digital Circuits Laboratory

Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Problem set: 5 Date: September 8, 2023

Instructions:

1. Use Behavioral and Dataflow modelling for this experiment.
2. Perform RTL simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA.
4. Perform the scanchain to verify your design on Xen-10 Board.

Problem Statement

1. Describe the given ALU using VHDL. This ALU circuit performs various functions based on select lines.

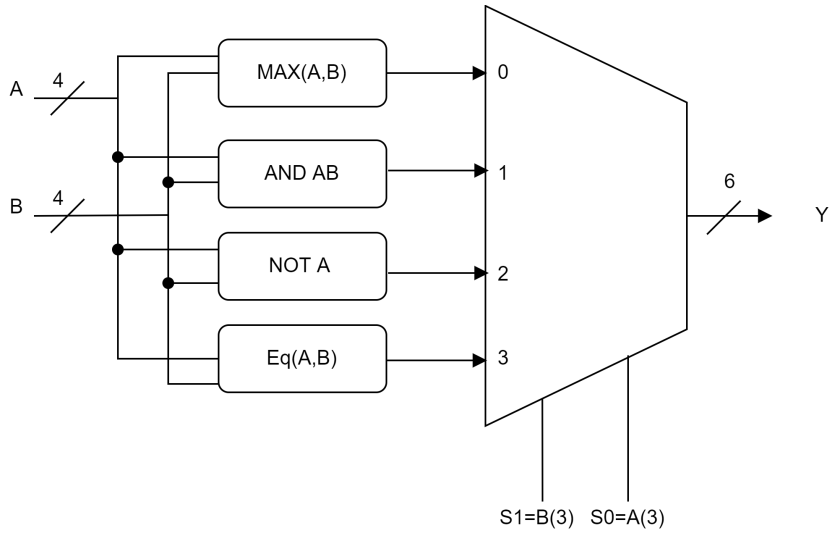

Figure 1: ALU with 4 functions

S1 S0	ALU Output
0 0	MAX(A,B): This block outputs larger number between A and B else outputs 0000.
0 1	AND A B: This block performs AND operation between A , B.
1 0	NOT A: This block performs NOT operation of A.
1 1	Eq(A,B): This block outputs the number whenever A=B else it should output 0000.

- In this problem MSB of inputs A and B are also working as selection lines. S1 is connected to MSB of input B [i.e. B(3)] and S0 is connected to MSB of input A [i.e. A(3)].
- Simulate your design using the generic testbench to confirm the correctness of your description.
- Tracefile format $< A3\,A2\,A1\,A0\,B3\,B2\,B1\,B0 > < Y5\,Y4\,Y3\,Y2\,Y1\,Y0 >$ 111111

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity alu_beh is
    port (
        A: in std_logic_vector(3 downto 0);
        B: in std_logic_vector(3 downto 0);
        sel: in std_logic_vector(1 downto 0);
        op: out std_logic_vector(7 downto 0)
    ) ;
end alu_beh;

architecture a1 of alu_beh is

    function sub(A: in std_logic_vector(3 downto 0); B: in std_logic_vector(3 downto 0))
        return std_logic_vector is
            -- declaring and initializing variables using aggregates
            variable diff : std_logic_vector(.....):=(others =>'0');
            variable carry: std_logic_vector(.....):=(others =>'0');
        begin
            -- Hint: Use for loop to calculate value of "diff" and "carry" variable
            -- Use aggregates to assign values to multiple bits
            return diff;
    end sub;

begin
alu : process( A, B, sel )
begin
    -- complete VHDL code for various outputs of ALU based on select lines
   -- Hint: use if/else statement
   --
   -- sub function usage :
   --   signal_name <= sub(A,B)
   --   variable_name := sub(A,B)
   --
   -- concatenate operator usage:
   --    "0000" & A
end process ; --alu
end a1 ; -- a1
```